

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for processing transmission control protocol (TCP) packets using hardware-based multi-threading techniques. Inbound and outbound TCP packet are processed using a multi-threaded TCP offload engine (TOE). The TOE includes an execution core comprising a processing engine, a scheduler, an on-chip cache, a host memory interface, a host interface, and a network interface controller (NIC) interface. In one embodiment, the TOE is embodied as a memory controller hub (MCH) component of a platform chipset. The TOE may further include an integrated direct memory access (DMA) controller, or the DMA controller may be embodied as separate circuitry on the MCH. In one embodiment, inbound packets are queued in an input buffer, the headers are provided to the scheduler, and the scheduler arbitrates thread execution on the processing engine. Concurrently, DMA payload data transfers are queued and asynchronously performed in a manner that hides memory latencies. In one embodiment, the technique can process typical-size TCP packets at 10 Gbps or greater line speeds.